A Realization Methodology of Emerging Various Types of Power Gated Circuits

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Abstract
High leakage current in deep-sub micrometer designs have become a significant contributor to total power dissipation of CMOS circuits, as short-channel transistors require lower power supply levels to reduce power consumption. This forces a reduction in the threshold voltage that causes a substantial increase of weak inversion current. As long power circuits are most popular now a days as the scaling increase the leakage powers in the circuit also increases rapidly so for removing these kind of leakages and to provide a better power efficiency we are using many types of power gating techniques. In this paper we are going to analyze the different types of flip-flops using different types of power gated circuits using low power VLSI design techniques and we are going to display the comparison results between different nanometre technologies. The simulations were done using Micro wind Layout Editor & DSCH software and the results were given below.

Keywords
Leakage Reduction, Low Power, Power Gating, Design Methodology

I. Introduction
Historically, power has been one of the primary drivers of the evolution of modern electronic devices: from vacuum tubes (1906, Le De Forest) to transistors (1947, William Shockley), from BJTs (bipolar transistors) to FETs (field effect transistors), and from MOSFET (metal-oxide-semiconductor field-effect transistor) to CMOS (complementary metal-oxide-silicon) MOSFET. Moreover, as the scale of integration expands, more transistors [1], faster and smaller than their predecessors, are being packed into smaller chips and the steady growth in clock frequency and processing capacity per chip has dramatically increased power consumption. As the power consumption becomes critical, the chip designer should consider the power sources and the power reduction methods in a more detailed manner than before, especially for leakage power because technology scaling results in leakage power increases. With respect to total power consumption [2-3], leakage power has increased from an almost negligible level to nearly 20 percent in 130-nanometre (nm) designs, 40 percent in 90-nm designs, and over 50 percent in 65-nm designs.

Now, managing leakage power effectively is critical to the success of VLSI chip design, especially for mobile applications. Several techniques have been proposed to reduce leakage power such as dual-Vth [4], mixed-Vth [5], Off-off MOS stacking [6], input-vector control [7], multi-threshold (MT) CMOS [8], selective MTCMOS (SMT) [9], Zigzag super cut-off CMOS (ZSCCMOS), optimal Zigzag CMOS (OZ), body-bias control, transistor width sizing, transistor channel scaling, and voltage islands. Among the leakage-control techniques, power gating is one of the most effective ways to lower the leakage of a VLSI circuit in the leakage dominant era. Power-gating uses a PMOS transistor or an NMOS transistor to disconnect the circuit’s supply voltage from the logic when the logic is inactive. This technique can reduce leakage by more than two orders of magnitude with negligible speed degradation [10].

The scaling of process technologies to nanometre regime has resulted in a rapid increase in leakage power dissipation. Hence, it has become extremely important to develop design techniques to reduce static power dissipation during periods of inactivity. The power reduction must be achieved without trading-off performance which makes it harder to reduce leakage during normal (runtime) operation. On the other hand, there are several techniques for reducing leakage power in sleep or standby mode. Power gating is one such well known technique where a sleep transistor is added between actual ground rail and circuit ground (called virtual ground). This device is turned-off in the sleep mode to cut-off the leakage path. It has been shown that this technique provides a substantial reduction in leakage at a minimal impact on performance Power gating technique uses high Vt sleep transistors which cut off VDD from a circuit block when the block is not switching. The sleep transistor sizing is an important design parameter. This technique, also known as MTCMOS, or Multi-Threshold CMOS reduces stand-by or leakage power, and also enables Idq testing.

Power gating affects design architecture more than clock gating. It increases time delays as power gated modes have to be safely entered and exited. Architectural trade-offs exist between designing for the amount of leakage power saving in low power modes and the energy dissipation to enter and exit the low power modes. Shutting down the blocks can be accomplished either by software or hardware. Driver software can schedule the power down operations. Hardware timers can be utilized [11-13].

A dedicated power management controller is another option. An externally switched power supply is a very basic form of power gating to achieve long term leakage power reduction. To shut off the block for small intervals of time, internal power gating is more suitable. CMOS switches that provide power to the circuitry are controlled by power gating controllers. Outputs of the power gated block discharge slowly. Hence output voltage levels spend more time in threshold voltage level. This can lead to larger short circuit current.

Power gating uses low-leakage PMOS transistors as header switches to shut off power supplies to parts of a design in standby or sleep mode. NMOS footer switches can also be used as sleep transistors. Inserting the sleep transistors splits the chip’s power network into a permanent power network connected to the power supply and a virtual power network that drives the cells and can be turned off. The quality of this complex power network is critical to the success of a power-gating design. Two of the most critical parameters are the IR-drop and the penalties in silicon area and routing resources. Power gating can be implemented using cell- or cluster-based (or fine grain) approaches or a distributed coarse-grained approach.
The size of the gate control is designed considering the worst case scenario that will require the circuit to switch during every clock cycle, resulting in a huge area impact. Some of the recent designs implement the fine-grain power gating selectively, but only for the low Vt cells. If the technology allows multiple Vt libraries, the use of low Vt devices is minimum in the design (20%), so that the area impact can be reduced. When using power gates on the low Vt cells the output must be isolated if the next stage is a high Vt cell. Otherwise it can cause the neighboring high Vt cell to have leakage when output goes to an unknown state due to power gating.

Gate control slew rate constraint is achieved by having a buffer distribution tree for the control signals. The buffers must be chosen from a set of always on buffers (buffers without the gate control signal) designed with high Vt cells [15]. The inherent difference between when a cell switches off with respect to another, minimizes the rush current during switch-on and switch-off.

Usually the gating transistor is designed as a high Vt device. Coarse-grain power gating offers further flexibility by optimizing the power gating cells where there is low switching activity. Leakage optimization has to be done at the coarse grain level, swapping the low leakage cell for the high leakage one. Fine-grain power gating is an elegant methodology resulting in up to 10 times leakage reduction. This type of power reduction makes it an appealing technique if the power reduction requirement is not satisfied by multiple Vt optimization alone.

**B. Coarse-Grain Power Gating**

The coarse-grained approach implements the grid style sleep transistors which drives cells locally through shared virtual power networks. This approach is less sensitive to PVT variation, introduces less IR-drop variation, and imposes a smaller area overhead than the cell- or cluster-based implementations. In coarse-grain power gating, the power-gating transistor is a part of the power distribution network rather than the standard cell. There are two ways of implementing a coarse-grain structure: Ring-based: The power gates are placed around the perimeter of the module that is being switched-off as a ring. Special corner cells are used to turn the power signals around the corners. Column-based: The power gates are inserted within the module with the cells abutted to each other in the form of columns. The global power is the higher layers of metal, while the switched power is in the lower layers.

Gate sizing depends on the overall switching current of the module at any given time. Since only a fraction of circuits switch at any point of time, power gate sizes are smaller as compared to the fine-grain switches. Dynamic power simulation using worst case
vectors can determine the worst case switching for the module and hence the size [16]. The IR drop can also be factored into the analysis. Simultaneous switching capacitance is a major consideration in coarse-grain power gating implementation. In order to limit simultaneous switching, gate control buffers can be daisy chained, and special counters can be used to selectively turn on blocks of switches.

III. Power Gating for Delay Reduction

![Fig. 3: Device with Power Gating with Reduced Area & Power Using Clustering Network Formation](image)

This work presented a logic clustering based solution to the problem of controlling/optimizing the power gating parameters. The key design considerations in the power mode transitions are minimizing the wakeup delay, the peak current, and the total size of sleep transistors. This work analyzed the relations between the three parameters, and solved the problem of finding logic clusters and their wakeup schedule that minimize the wakeup delay while satisfying the peak current and performance loss constraints.

![Fig. 4: Sleepy Stack](image)

A variation of the sleep approach, the zigzag approach, reduces wake-up overhead caused by sleep transistors by placement of alternating sleep transistors assuming a particular pre-selected
input vector [6]. Another technique for leakage power reduction is the stack approach, which forces a stack effect by breaking down an existing transistor into two half size transistors [7]. The divided transistors increase delay significantly and could limit the usefulness of the approach. The sleepy stack approach fig. 2, combines the sleep and stack approaches [2-3]. The sleepy stack technique divides existing transistors into two half size transistors like the stack approach. Then sleep transistors are added in parallel to one of the divided transistors. During sleep mode, sleep transistors are turned off and stacked transistors suppress leakage current while saving state. Each sleep transistor, placed in parallel to the one of the stacked transistors, reduces resistance of the path, so delay is decreased during active mode. However, area penalty is a significant matter for this approach since every transistor is replaced by three transistors and since additional wires are added for S and S', which are sleep signals. Another technique called Dual sleep approach [8] fig. 3, uses the advantage of using the two extra pull-up and two extra pull-down transistors in sleep mode either in OFF state or in ON state. Since the dual sleep portion can be made common to all logic circuitry, less number of transistors is needed to apply a certain logic circuit. The differences between these three power gating techniques are checked by designing a flip-flop’s then simulated using the tools and snapshots are given below are given below. As flip-flops are most commonly used in all the digital circuits it is much needed to make the flip-flops much power efficient than all other devices. In this Part we are designing the low power flip-flops by reducing the power using power gated technology. The new flip-flop design’s using Dual Stack method is shown below. The dual stack method has noise efficiency & power efficiency than normal flip-flops.

Fig. 8: SCCER Flip-Flop Using Power Gated Circuits

IV. Tabulation Results

<table>
<thead>
<tr>
<th>Type</th>
<th>Area</th>
<th>Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>CDMFF</td>
<td>390um</td>
<td>0.271mW</td>
</tr>
<tr>
<td>CDMFF with Dual Stack</td>
<td>630um</td>
<td>0.185mW</td>
</tr>
<tr>
<td>SCCER</td>
<td>380um</td>
<td>6.929uW</td>
</tr>
<tr>
<td>SCCER with Dual Stack</td>
<td>704um</td>
<td>3.297uW</td>
</tr>
</tbody>
</table>

Thus the Dual stack method shows much reduced power than all the circuits. But the area constraints have been considerably increased. But using scaling techniques we can improve the area constraints.

V. Conclusion

We have addressed many of the considerations involved in the design of power gated circuits. In nanometre scale CMOS technology, sub threshold leakage power consumption is a great challenge. Although previous approaches are effective in some ways, no perfect solution for reducing leakage power consumption is yet known. Therefore, designers choose techniques based upon technology and design criteria. In this paper, we provide novel circuit structure named “Dual stack” as a new remedy for designers in terms of static power and dynamic powers. Unlike the sleep transistor technique, the dual stack technique retains the original state. The dual stack approach shows the least speed power product among all methods. Therefore, the dual stack technique provides new ways to designers who require ultra-low leakage power consumption with much less speed power product. Especially it shows nearly 50-60% of power than the existing normal or conventional flip-flops. So, it can be used for future integrated circuits for power & area Efficiency.
References


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